TFA9873_SDS

High-efficiency Class-D Audio Amplifier

Version: 1.2

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Contents

1 General description

The TFA9873 is a high-efficiency boosted class-D audio amplifier. It can deliver up to 4.5 W average output power into a 6 Ω speaker, at a supply voltage of 4.0 V (THD = 1 %). The internal adaptive DC-to-DC converter raises the supply voltage, providing ample headroom for major improvements in sound quality.

Internal adaptive DC-to-DC conversion boosts the supply rail to provide additional headroom and power output. The supply voltage is only raised when necessary. So, it maximizes the output power of the class-D audio amplifier while limiting quiescent power consumption.

The TFA9873 can be configured to drive either a hands-free speaker (4 Ω to 8 Ω) for audio playback or a receiver speaker upto (32 Ω) for handset playback. So, it can be embedded in platforms supporting both a hands-free speaker and a handset speaker. The maximum output power and the noise levels are lower in handset call use case than in hands-free call use case.

The TFA9873 also incorporates battery protection. By limiting the supply current when the battery voltage is low, it prevents the audio system from drawing excessive load currents from the battery, which can cause a system under voltage. This circuitry minimizes the impact of a falling battery voltage by preventing unexpected device switch off due to excessive current drawn from the battery.

The device features low RF susceptibility because it has a digital input interface that is insensitive to clock jitter. The second order closed loop architecture used in a class-D audio amplifier provides excellent audio performance and high supply voltage ripple rejection. The audio input interface is TDM and the control settings are communicated via an I^2C-bus interface.

The TFA9873 is available in a 30-bump wafer level chip-size package (WLCSP) with a 400 µm pitch.

2 Features and benefits

- High output power:
  - 4.5 W (average) into 6 Ω at 4.0 V supply voltage (THD = 1 %)
  - 3.5 W (average) into 8 Ω at 4.0 V supply voltage (THD = 1 %)
- Supports handset (16 Ω or 32 Ω) and hands-free (4 Ω to 8 Ω) speaker configurations
- High efficiency, low power dissipation, and low-noise speaker driver
- Adaptive DC-to-DC converter increases the supply voltage smoothly when switching between fixed boost and adaptive boost modes, preventing large battery supply spikes and limiting quiescent power consumption
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V)
- Very low-noise output voltage, 9 µV
- Low battery current consumption, 120 mA (P_o = 380 mW, average music power)
- I^2C-bus control interface (400 kHz)
- Speaker current and voltage monitoring (via the TDM-bus) for acoustic echo cancellation (AEC) at the host
- 16 kHz/32 kHz/44.1 kHz/48 kHz sample frequencies supported
- Ultrasonic support via TDM running at 96 kHz
- Programmable interrupt control via a dedicated interrupt pin
- Low RF susceptibility
- Thermal foldback and overtemperature protection

3 Applications

- Mobile phones and tablets
- Portable navigation devices (PND)

4 Quick reference data

Table 4-1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT; V_{BAT} must not be lower than V_{DDD} in application.	2.7	-	5.5	V
V_{DDD}	digital supply voltage	on pin VDDD	1.65	1.8	1.95	V
$V_{DD(IO)}$	IO interface supply voltage	on pin VDD(IO)	1.65	-	3.6	V
R_L	load resistance		3.2	-	38	Ω
I_{BAT}	battery supply current	normal power mode; operating mode with load R_L = 6 Ω; P_o = 380 mW (average music power) V_{BAT} = 4.0 V; V_{BST} = 8 V; $V_{DD(IO)}$ = V_{DDD} = 1.8 V;	-	120	-	mA
		low-power mode; amplifier switching input signal detection active P_o = 0 mW; V_{BAT} = 4.0 V; V_{BST} = 8 V; $V_{DD(IO)}$ = V_{DDD} = 1.8 V;	-	3.8	-	mA
		idle power mode; amplifier ready to receive signal, input signal detection active P_o = 0 mW	-	55	-	µA
		power-down state; on pin VBAT; DC-to-DC in power-down mode; T_j = 25 °C	-	1	-	µA
I_{DDD}	digital supply current	normal power mode; operating mode with load R_L = 6 Ω; P_o = 380 mW (average music power); V_{BAT} = 4.0 V; V_{BST} = 8 V; $V_{DD(IO)}$ = V_{DDD} = 1.8 V	-	6.6	-	mA
		low-power mode; amplifier switching input signal detection active; P_o = 0 mW; V_{BAT} = 4.0 V; V_{BST} = 8 V; $V_{DD(IO)}$ = V_{DDD} = 1.8 V	-	5.1	-	mA
		idle power mode; amplifier ready to receive signal; input signal detection active; P_o = 0 mW	-	3	-	mA
		power-down state	-	1.5	19	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{o(AV)}$	average output power	THD+N = 1 % (R_L = 8 Ω; L_L = 44 µH); V_{BST} = 8.0 V; V_{BAT} = 4.0 V; $V_{DD(IO)}$ = V_{DDD} = 1.8 V	3.3	3.5	-	W
		THD+N = 1 % (R_L = 6 Ω; L_L = 32 µH); V_{BST} = 8.0 V; V_{BAT} = 4.0 V; $V_{DD(IO)}$ = V_{DDD} = 1.8 V	4.2	4.5	-	W
		THD+N = 1 %; (R_L = 4 Ω; L_L = 22 µH); V_{BST} = 7.0 V; V_{BAT} = 4.0 V; $V_{DD(IO)}$ = V_{DDD} = 1.8 V	-	4.7	-	W

5 Ordering information

Table 5-1: Ordering information

Type number	Package		
	Name	**Description**	**Version**
TFA9873DUK/N1	WLCSP30	wafer level chip-scale package; 30 bumps; 0.4 mm pitch, 2.42 mm × 2.18 mm × 0.5 mm; no back side coating	SOT1443-6
TFA9873EUK/N1	WLCSP30	wafer level chip-scale package; 30 bumps; 0.4 mm pitch, 2.42 mm × 2.18 mm × 0.525 mm; back side coating	SOT1443-7

6 Block diagram

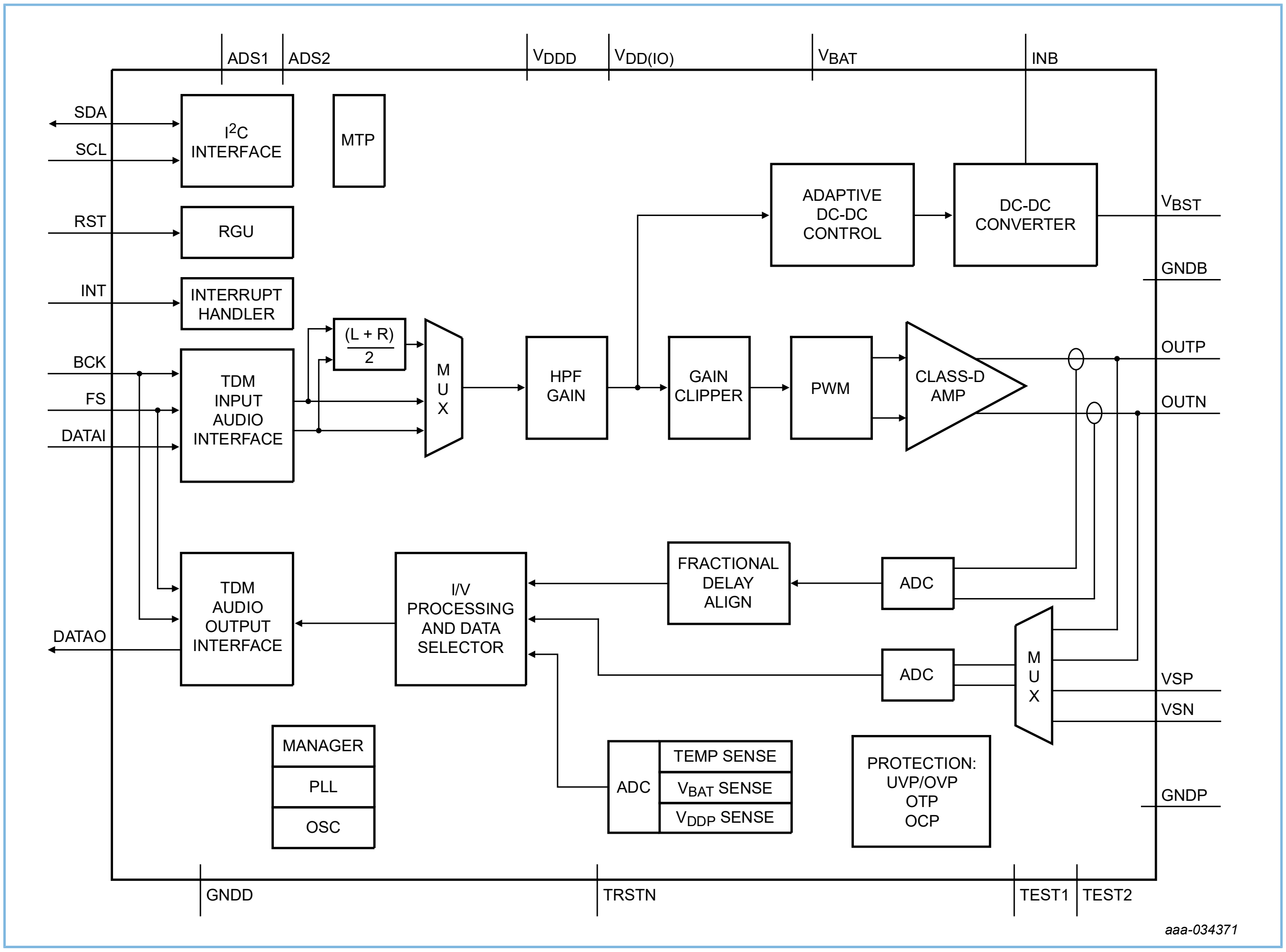


Figure 6-1: Block diagram

7 Pinning information

7.1 Pinning

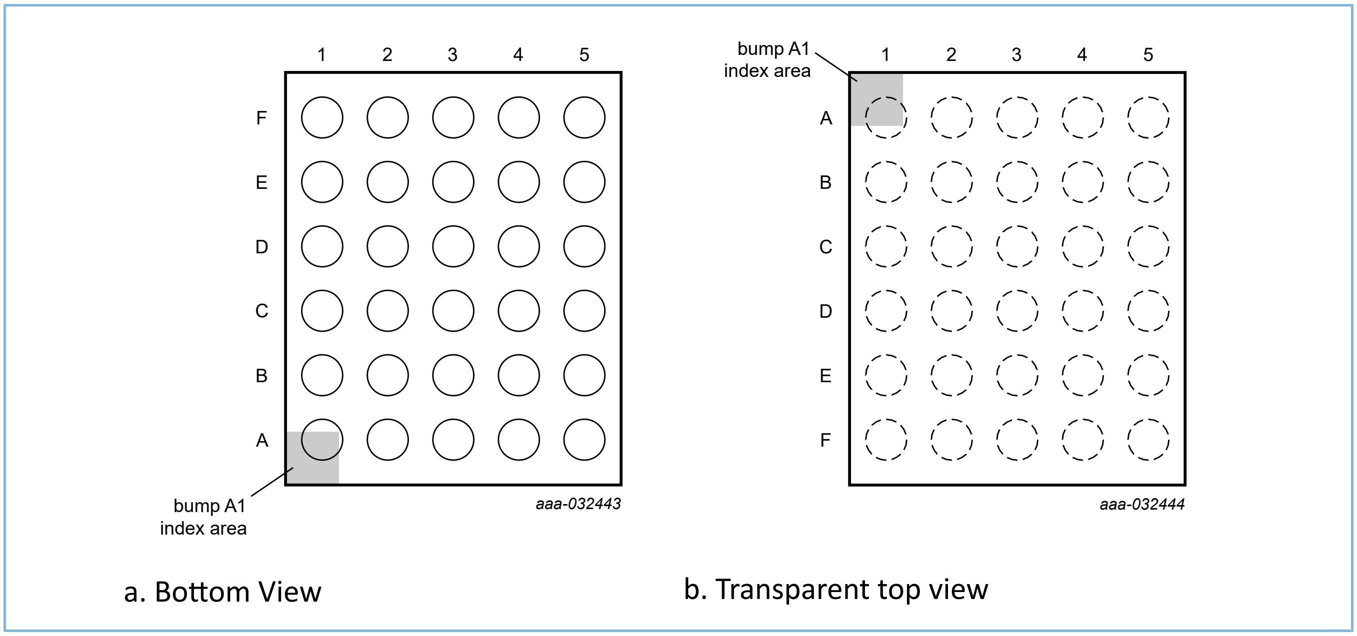


Figure 7-1: Bump configuration

	1	2	3	4	5
A	DATAI	BCK	FS	GNDP	OUTN
B	DATAO	RST	INT	GNDP	VBST
C	GNDD	GNDD	VSN	TEST1	OUTP
D	VDDD	ADS1	VSP	TEST2	VBST
E	VDD(IO)	ADS2	TRSTN	GNDB	INB
F	SCL	SDA	VBAT	GNDB	INB

aaa-032445

Figure 7-2: Bump mapping - Transparent top view

Table 7-1: Pinning

Symbol	Pin	Type	Description
DATAI	A1	I	digital audio data input for TDM interface
BCK	A2	I	digital audio bit clock input for TDM interface
FS	A3	I	digital audio frame sync input for TDM interface
GNDP	A4	P	power ground
OUTN	A5	O	inverting output

Symbol	Pin	Type	Description
DATAO	B1	O	digital audio data output for TDM interface
RST	B2	I	reset input
INT	B3	O	digital interrupt output
GNDP	B4	P	power ground
VBST	B5	P	boosted supply voltage output
GNDD	C1	P	digital ground
GNDD	C2	P	digital ground
VSN	C3	I	voltage sense negative input
TEST1	C4	I/O	test signal input 1; for test purposes only; connect to PCB ground
OUTP	C5	O	non-inverting output
VDDD	D1	P	digital supply voltage
ADS1	D2	I	digital address select input 1
VSP	D3	I	voltage sense positive input
TEST2	D4	I/O	test signal input 2; for test purposes only; connect to PCB ground
VBST	D5	P	boosted supply voltage output
VDD(IO)	E1	P	IO interface supply voltage
ADS2	E2	I	digital address select input 2
TRSTN	E3	I	test reset input ; for test purposes only; connect to PCB ground
GNDB	E4	P	boosted ground
INB	E5	P	DC-to-DC boost converter input
SCL	F1	I	digital I^2C-bus clock input
SDA	F2	I/O	digital I^2C-bus data input
VBAT	F3	P	battery supply voltage
GNDB	F4	P	boosted ground
INB	F5	P	DC-to-DC boost converter input

8 Functional description

The TFA9873 is a highly efficient bridge-tied load (BTL) class-D audio amplifier as depicted in block diagram (see Figure 6-1).

TFA9873 contains a TDM input/output interface for communicating with the audio host. It also offers the possibility of providing an ultrasonic path to the speaker.

At low battery voltage levels, the gain (from TDM interface to speaker output) is automatically reduced to limit battery current (when battery safeguard is enabled).

The digital audio stream is converted into two pulse-width modulated (PWM) signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

An adaptive DC-to-DC converter boosts the output voltage to the level the class-D amplifier requires.

9 I^2C-bus interface and register settings

The TFA9873 supports the 400 kHz I^2C-bus microcontroller interface mode standard. The I^2C-bus is used to control the TFA9873 and to transmit and receive data. The TFA9873 can only operate in I^2C slave mode, as a slave receiver or as a slave transmitter.

10 Limiting values

Table 10-1: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT		−0.3	-	+6	V
V_{BST}	booster output voltage	on pin VBST	[1]	−0.3	-	+9.6	V
V_{INB}	booster input voltage	on pin INB	[1]	−0.3	-	+9.6	V
V_O	output voltage	on speaker connections; pins OUTP, OUTN	[1]	−0.3	-	+9.6	V
V_{DDD}	digital supply voltage	on pin VDDD		−0.3	-	+2.5	V
$V_{DD(IO)}$	IO interface supply voltage	on pin VDD(IO)		−0.3	-	+4.6	V
V_{low}	low voltage	on pins TEST1/TEST2		−0.3	-	+2.5	V
T_j	junction temperature			-	-	125	°C
T_{stg}	storage temperature			−55	-	+150	°C
T_{amb}	ambient temperature			−40	-	+85	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM)		−2	-	+2	kV
		Charge Device Model (CDM)		−500	-	+500	V

[1] Using the Goodix Technology demo board, with a 1 mm wire/PCB track length on INB pin, AC pulses between −6 V and +12 V can be observed without damaging the device. These spikes do not end up inside the actual device.

11 Thermal characteristics

Table 11-1: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	4-layer application board	60	-	K/W

12 Characteristics

12.1 DC characteristics

Table 12-1: DC characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; $V_{DD(IO)}$ = V_{DDD} = 1.8 V; V_{BST} = 8.0 V, adaptive boost mode; L_{BST} = 1 μH[1]; R_L = 8 Ω[1]; L_L = 44 μH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT; V_{BAT} must not be lower than V_{DDD}		2.7	-	5.5	V
I_{BAT}	battery supply current	normal power mode; operating mode with load R_L = 6 Ω; P_o = 380 mW (average music power)		-	120	-	mA
		low-power mode; amplifier switching; input signal detection active; P_o = 0 mW		-	3.2	-	mA
		idle power mode; amplifier ready to receive signal; input signal detection active; P_o = 0 mW		-	55	-	μA
		power-down state; on pin VBAT; DC-to-DC in power-down mode; T_j = 25 °C; no clock		-	1	-	μA
V_{DDD}	digital supply voltage	on pin VDDD		1.65	1.8	1.95	V
I_{DDD}	digital supply current	normal power mode; operating mode with load R_L = 6 Ω; P_o = 380 mW (average music power)		-	5.5	-	mA
		low-power mode; amplifier switching; input signal detection active; P_o = 0 mW		-	4.4	-	mA
		idle power mode; amplifier ready to receive signal, input signal detection active P_o = 0 mW		-	2.6	-	mA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		power-down state		-	1.5	19	µA
$V_{DD(IO)}$	IO interface supply voltage	on pin VDD(IO)		1.65	-	3.6	V
Pins SCL and SDA							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	$V_{DD(IO)}$	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(IO)}$	V
Pins FS, BCK, DATAI, ADS1, ADS2, RST							
V_{IH}	HIGH-level input voltage			$0.65V_{DD(IO)}$	-	$V_{DD(IO)}$	V
V_{IL}	LOW-level input voltage			-	-	$0.35V_{DD(IO)}$	V
C_{in}	input capacitance		[2]	-	-	5	pF
I_{LI}	input leakage current	1.8 V on input pin FS, BCK, DATAI, ADS1, ADS2, SCL, SDA		-	-	0.12	µA
		1.8 V on input pin TRSTN, pulldown current		-	20	-	µA
		1.8 V on input pin RST, pulldown current		-	90	=	µA
Pins DATAO, INT, push-pull output stages							
V_{OH}	HIGH-level output voltage			$V_{DD(IO)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage			-	-	400	mV
Pins SDA, open-drain outputs, external 10 kΩ resistor to $V_{DD(IO)}$							
V_{OH}	HIGH-level output voltage			$V_{DD(IO)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	400	mV
Pins OUTP, OUTN							
R_{DSon}	drain-source on-state resistance	PMOS + NMOS transistors		-	400	500	mΩ
Protections							
$T_{act(th\_prot)}$	thermal protection activation temperature			130	-	-	°C
$V_{ovp(VBST)}$	overvoltage protection on pin VBST			9.0	-	9.6	V
$V_{uvp(VBAT)}$	undervoltage protection on pin VBAT			2.3	-	2.7	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{O(ocp)}$	overcurrent protection output current			2.2	-	-	A
DC-to-DC converter							
V_{BST}	voltage on pin VBST	DCVOS = 101111; boost mode (after trim)	[3]	7.9	8	8.1	V

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production. The value is guaranteed by design and checked during product validation.
[3] Boost switching frequency = 2 MHz in PWM mode.

12.2 AC characteristics

Table 12-2: AC characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; $V_{DD(IO)}$ = V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 8.0 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω [1] ; L_L = 44 µH[1] ; f_i = 1 kHz; f_s = 48 kHz; f_{pwm} = 384 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier output power							
$P_{o(AV)}$	average output power	hands-free speaker; THD+N = 1 %; V_{DDD} = 1.8 V					
		R_L = 8 Ω; L_L = 44 µH		3.3	3.5	-	W
		R_L = 6 Ω; L_L = 32 µH		4.2	4.5	-	W
		R_L = 4 Ω; L_L = 22 µH; V_{BST} = 7.0 V		-	4.7	-	W
		receiver speaker; THD+N = 1 %; V_{BST} = 8.0 V					
		R_L = 32 Ω; voice mode		-	0.2	-	W
		R_L = 32 Ω; audio mode		-	0.9	-	W
Amplifier output pins (OUTP and OUTN)							
$\|V_O(offset)\|$	output offset voltage	absolute value; after trimming; V_{DDP} = 3.4 V to 8.0 V; V_{BAT} = 3.4 V to 5 V		-	-	1.0	mV
Amplifier performances							
η_{po}	output power efficiency	on pin VBAT; operating mode with load R_L = 6 Ω; L_L = 32 µH; P_o = 380 mW (average music power); f_{sw} = 768 kHz	[2]	-	80	-	%

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		on pin VBAT; operating mode with load R_L = 6 Ω; L_L = 32 µH; P_o = 380 mW (average music power)	[2]	-	82	-	%
		on pin VBAT; input: 100 Hz sine wave; R_L = 8 Ω; L_L = 44 µH; P_o = 700 mW	[2]	-	91	-	%
		on pin VBAT; input: 100 Hz sine wave; R_L = 8 Ω; L_L = 44 µH; P_o = 3 W; f_{pwm} = 768 kHz	[2]	-	82	-	%
		on pin V_{BAT}; input: 100 Hz sine wave; R_L = 8 Ω; L_L = 44 µH; P_o = 3 W	[2]	-	89	-	%
THD+N	total harmonic distortion-plus-noise	P_o = 2.0 W; R_L = 8 Ω; L_L = 44 µH	[1]	-	-	0.05	%
		P_o = 2.0 W; R_L = 4 Ω; L_L = 20 µH	[1]	-	-	0.09	%
$V_{n(o)}$	output noise voltage	a-weighted; no input signal; normal mode; f_{pwm} = 768 kHz; f_s = 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz	[2]	-	25	-	µV
		a-weighted; no input signal; low-noise mode; f_{pwm} = 768 kHz; f_s = 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz	[2]	-	9	14	µV
		a-weighted; no input signal; normal mode; f_s = 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz	[2]	-	40	50	µV
		a-weighted; no input signal; low-noise mode; f_s = 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz	[2]	-	10	15	µV
		a-weighted; no input signal; idle power mode; f_s = 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz	[2]	-	1	-	µV
DR	dynamic range	a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at	[2]	109	113	-	dB

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		THD = 1 %); output noise voltage ($V_{n(o)}$); no signal applied					
S/N	signal-to-noise ratio	a-weighted, V_{BAT} = 3.4 V to 5 V; maximum signal at THD = 1 %	[2]	98	-	-	dB
PSRR	power supply rejection ratio	from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 217 Hz square wave; V_{ripple} = 50 $mV_{(p-p)}$; V_{BAT} = 4.0 V		70	85	-	dB
		from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 20 Hz to 1 kHz sine wave, V_{ripple} = 200 mV (RMS); V_{BAT} = 3.4 V to 5.0 V; low-power mode on; low-noise mode on		70	90	-	dB
		from V_{BAT}; booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 1 kHz to 20 kHz sine wave, V_{ripple} = 200 mV (RMS); V_{BAT} = 3.4 V to 5.0 V		55	60	-	dB
ΔG/Δf	gain variation with frequency	BW = 20 Hz to 15 kHz; V_{BAT} = 3.4 V to 5 V		−0.1	-	+0.7	dB
V_{POP}	pop noise voltage	at mode transition and gain change.		-	-	2	mV
R_L	load resistance			3.2	8	38	Ω
C_L	load capacitance			-	-	1	nF
f_{sw}	switching frequency	directly coupled to the TDM input frequency		352.8	-	768	kHz
$G_{(TDM-VO)}$	TDM to V_O gain	INPLEV = 0 dB		6	-	21	dB
Amplifier power-up, power-down, and propagation delays							
$t_{d(on)PLL}$	PLL turn-on delay time	PLL locked on BCK; f_s = 48 kHz		-	2	-	ms
$t_{d(on)amp}$	amplifier turn-on delay time	f_s = 48 kHz		-	55	-	µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(off)}$	turn-off delay time			-	32	-	µs
$t_{d(alarm)}$	alarm delay time			-	200	-	ms
t_{PD}	propagation delay	delta propagation delay between left and right in stereo application = 1.625 FS					
		f_s = 16 kHz		-	-	1	ms
		f_s = 32 kHz		-	-	750	µs
		f_s = 44.1 kHz		-	-	710	µs
		f_s = 48 kHz		-	-	700	µs
		f_s = 96 kHz		-	-	600	µs
Booster inductance							
L_{bst}	boost inductance			0.33	1	1.2	µH
Voltage and current sensing performance							
S/N	signal-to-noise ratio	I_O = 1.1 A (peak); a-weighted		62	65	-	dB
$\Delta V_{sense}/I_{sense}$	V_{sense}/I_{sense} ratio mismatch	pilot tone −40 dBFS	[3]	-	2	-	%
THD+N	total harmonic distortion-plus-noise	f_i = 20 Hz to 20 kHz; V_i = −12 dBFS		-	-	0.75	%

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production. The value is guaranteed by design and checked during product validation.
[3] Intended for Speaker protection. In combination with Goodix Speaker protection a speaker temperature accuracy of ±10 °C can be realized.

12.3 TDM timing characteristics

Table 12-3: TDM bus interface characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 8.0 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_s	sampling frequency	on pin WS; audio mode	[2]	16	-	48	kHz
		on pin WS; ultrasonic mode		-	-	96	kHz
f_{clk}	clock frequency	on pin BCK; audio mode	[2]	$32f_s$	-	$384f_s$	kHz
		on pin BCK; ultrasonic mode		-	-	$96f_s$	MHz
t_{su}	set-up time	WS edge to BCK HIGH	[3]	10	-	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		DATA edge to BCK HIGH		10	-	-	ns
t_h	hold time	BCK HIGH to WS edge	[3]	10	-	-	ns
		BCK HIGH to DATA edge		10	-	-	ns
t_J	external clock jitter	PLL locked on BCK	[4]	-	1	2	ns
		PLL locked on FS	[5]	-	-	20	ns

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] The TDM bit clock input (BCK) is used as a clock input for the amplifier and the DC-to-DC converter. The BCK and WS signals must be present for the clock to operate correctly.
[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.
[4] When the PLL is locked on BCK, amplifier output noise can deteriorate when clock jitter > 1 ns; performance is guaranteed up to jitter = 2 ns.
[5] The system is less sensitive to jitter when the PLL is locked on FS.

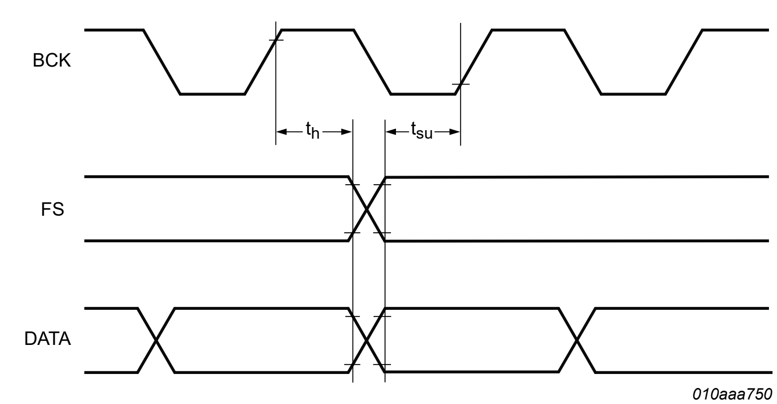


Figure 12-1: TDM timing

12.4 I²C timing characteristics

Table 12-4: I²C-bus interface characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 8.0 V, adaptive boost mode; L_{BST} = 1 μH[1]; R_L = 8 Ω[1]; L_L = 44 μH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	μs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	μs
t_r	rise time	SDA and SCL signals	[2]	$20 + 0.1C_b$	-	-	ns
t_f	fall time	SDA and SCL signals	[2]	$20 + 0.1C_b$	-	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{HD;STA}$	hold time (repeated) START condition		[3]	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[4]	0	-	50	ns
C_b	capacitive load for each bus line			-	-	400	pF

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
[3] After this period, the first clock pulse is generated.
[4] To be suppressed by the input filter.

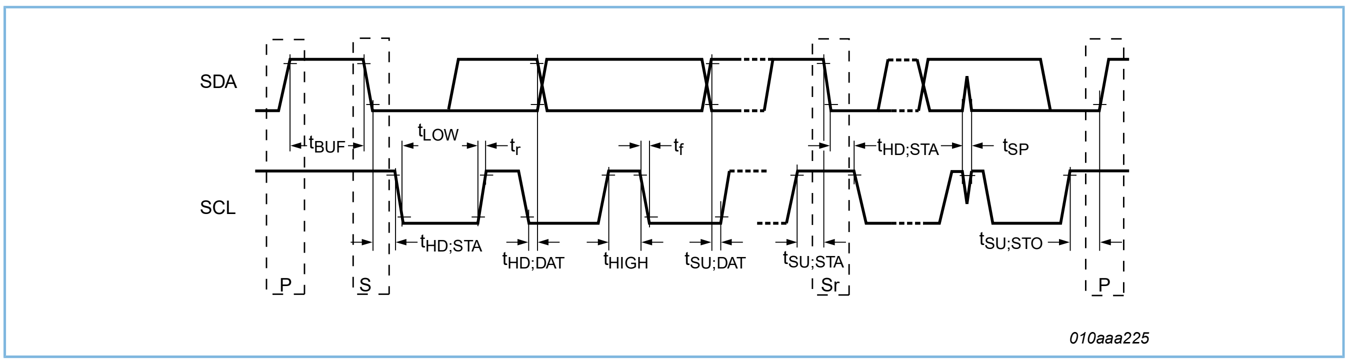


Figure 12-2: I²C timing

13 Application information

13.1 Application diagrams

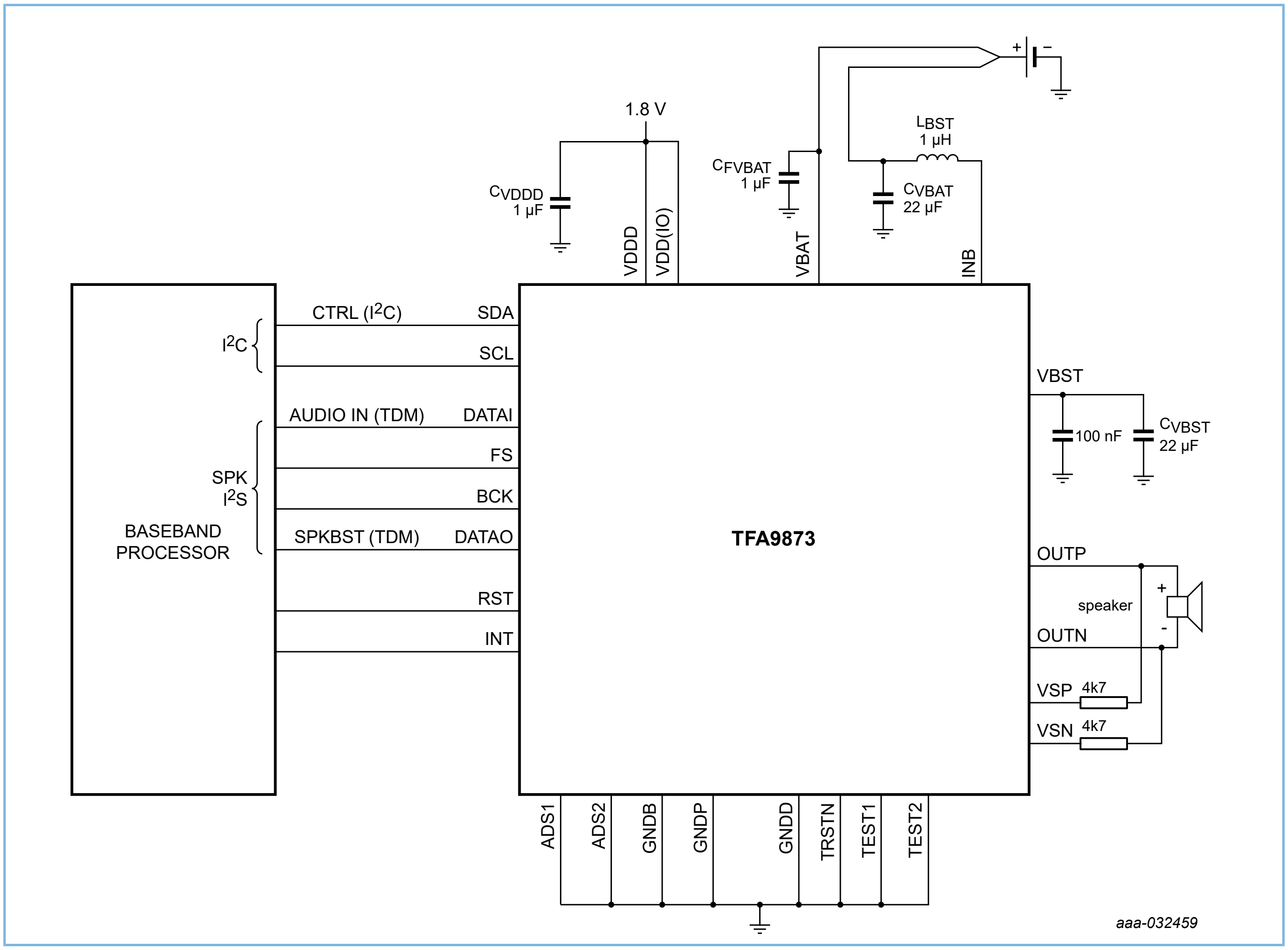


Figure 13-1: Typical mono application

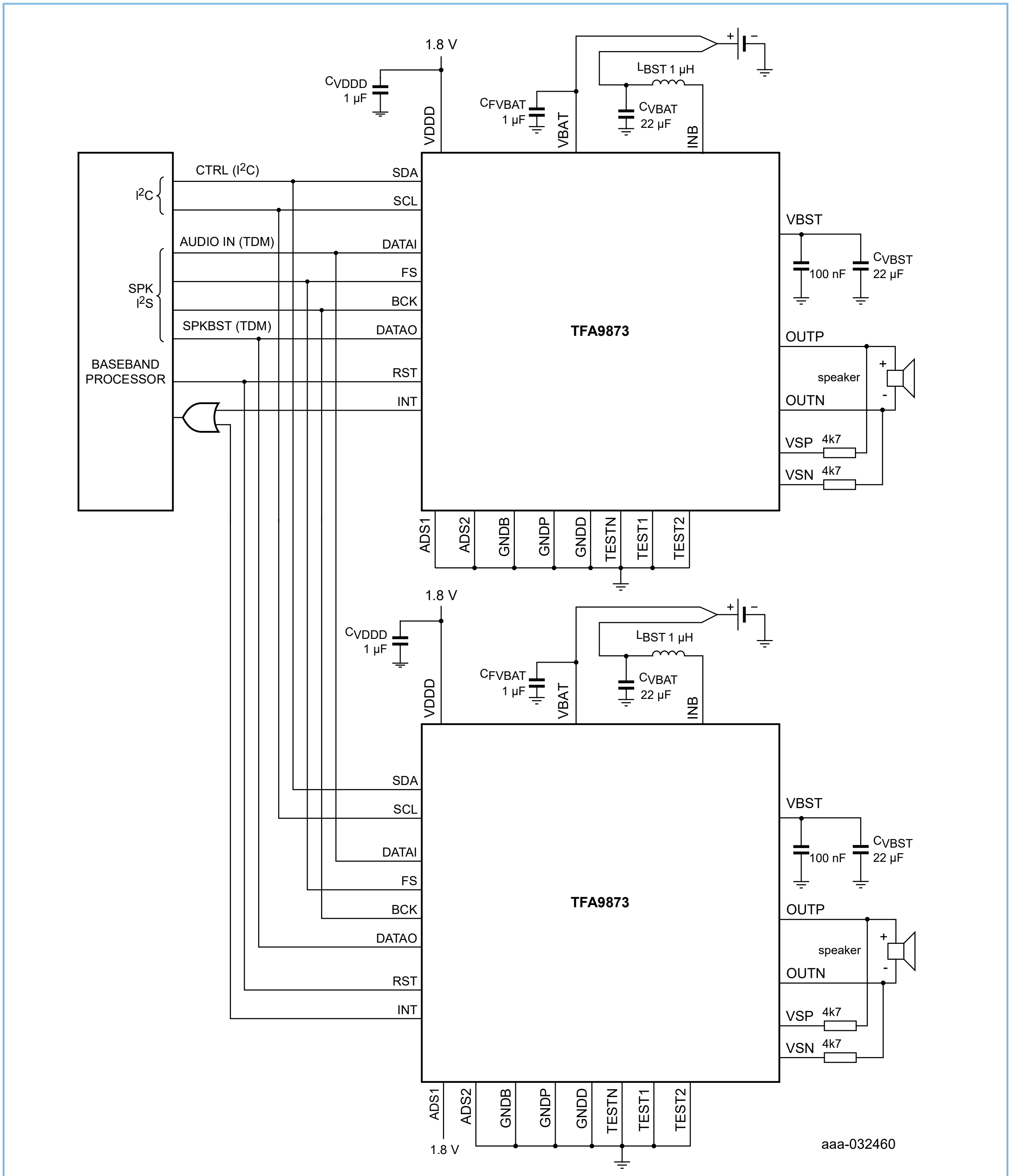


Figure 13-2: Typical stereo application

14 Package outline

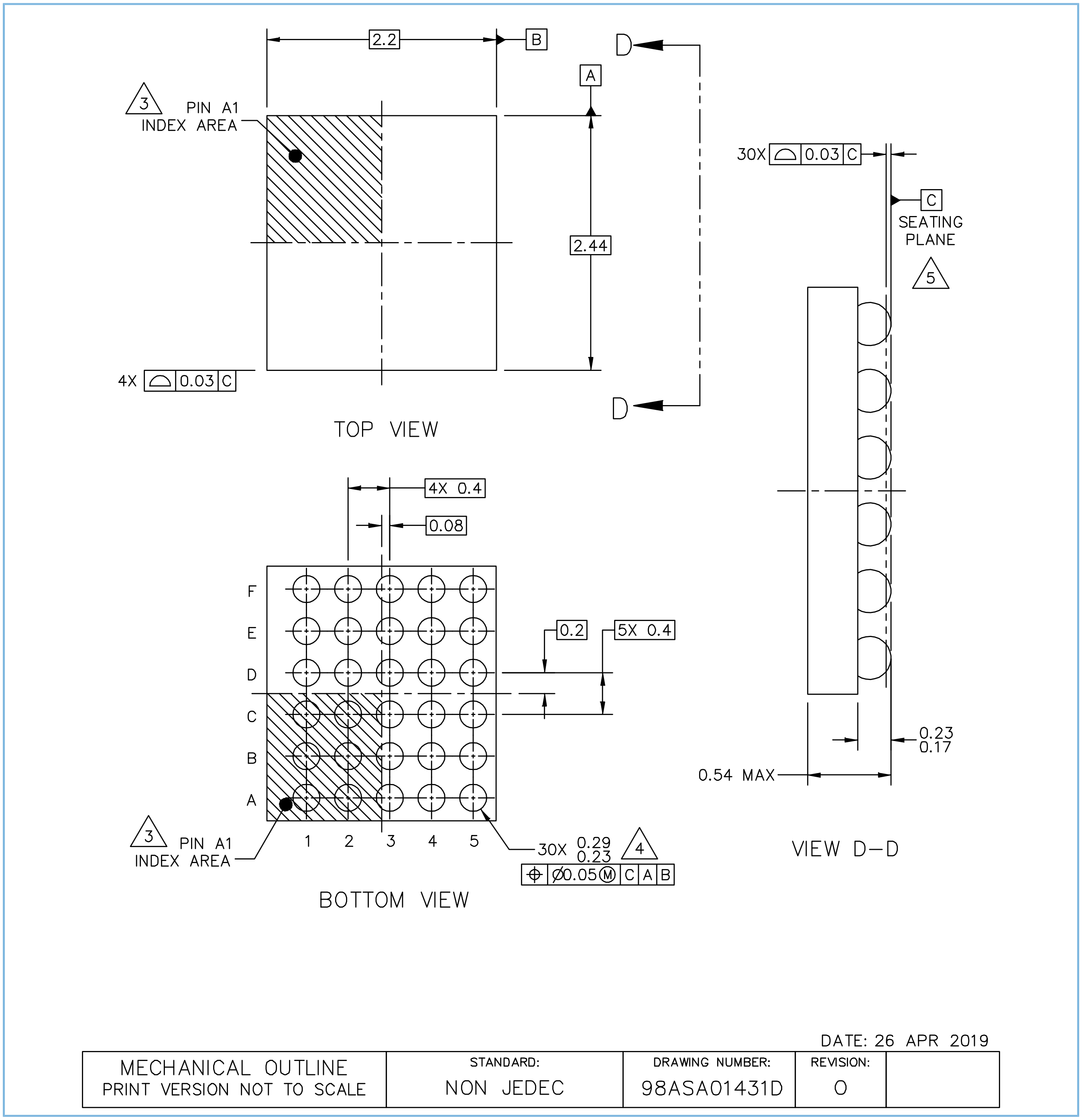


Figure 14-1: Package outline WLCSP30 (SOT1443-6); with back side coating

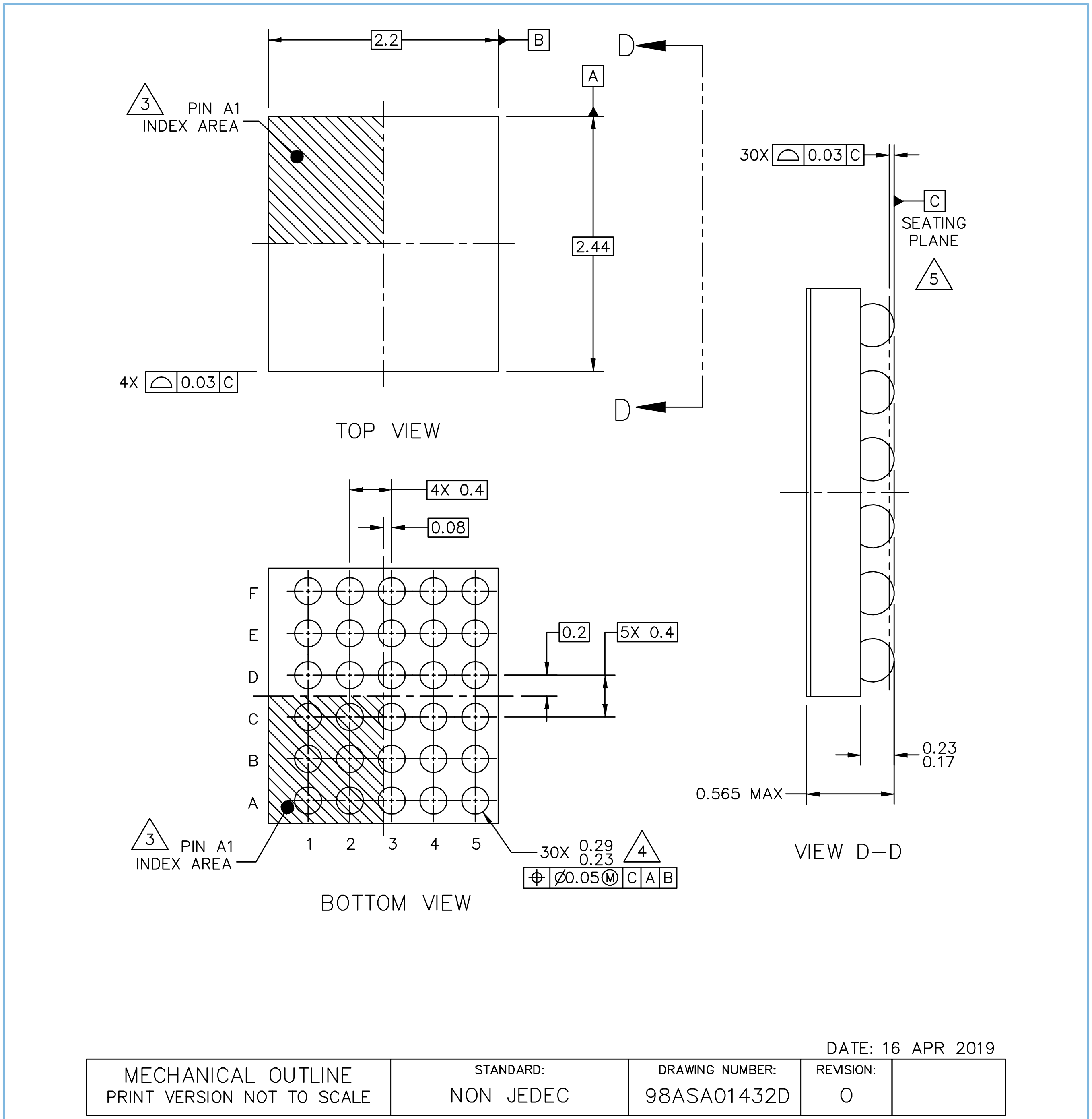


Figure 14-2: Package outline WLCSP30 (SOT1443-7); without back side coating

15 Soldering of WLCSP packages

15.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. More information about handling, packing, shipping and soldering of moisture/reflow sensitive surface-mount devices can be found in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

Wave soldering is not suitable for this package.

All Goodix Technology WLCSP packages are lead-free.

15.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

15.3 Reflow soldering

Key characteristics in reflow soldering are:

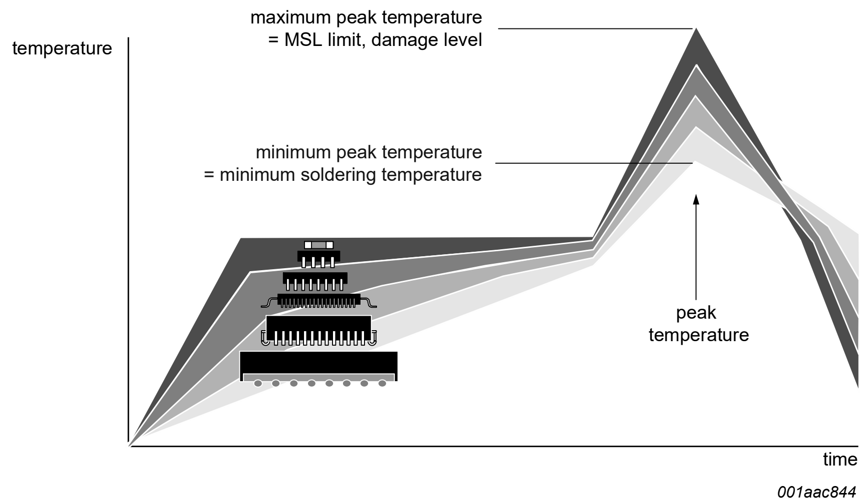
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 15-1) than a SnPb process, thus reducing the process window.
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board.
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15-1.

Table 15-1: Lead-free process (from J-STD-020D)

Package thickness (mm)	**Package reflow temperature (°C)**		
	Volume (mm^3)		
	< 350	**350 to 2 000**	**> 2 000**
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must always be respected.

Studies have shown that small packages reach higher temperatures during reflow soldering (see Figure 15-1).



MSL: Moisture Sensitivity Level

Figure 15-1: Temperature profiles for large and small components

For further information on temperature profiles, see the IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

15.3.1 Stand off

The standoff between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to thermal expansion coefficient (TEC) differences between substrate and chip.

15.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint must be smooth and the shape symmetrical. The soldered joints on a chip must be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures related to these voids have been found. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

15.3.3 Rework

In general, rework is not recommended. By rework, we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip are damaged. In that case it is recommended not to reuse the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate must be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side and on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

15.3.4 Cleaning

Cleaning can be done after reflow soldering.

16 Legal and contact information

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17 Revision history

Table 17-1: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9873_SDS v 1.2	20201210	Product short data sheet	-	TFA9873_SDS v 1.1
Modifications:	• Removed unnecessary logos			
TFA9873_SDS v 1.1	20201022	Product short data sheet	-	TFA9873_SDS v.1.0
Modifications:	• Updated to refelect TFA9873DS version 1.5			
TFA9873_SDS v 1.0	20200214	Product short data sheet	-	TFA9873_SDS v.0.2
Modifications:	• Updated document format based on Goodix template			
TFA9873_SDS v.0.2	20200120	Objective data sheet	-	-